University of Waterloo
ECE 439

Project Final Report

Design of a Ring Oscillator Based Voltage Controlled Oscillator

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1.0 Introduction

The project specifications are to design a voltage controlled oscillator (VCO) based on ring oscillators, which provides a frequency range from 1.884GHz to 1.9GHz. The voltage applied to the VCO is 1.8V. The power consumption of the whole oscillator should not exceed 18mW. The overall objective is to design a robust VCO with minimum power consumption and minimum consumed cell area. The design of the VCO must be in 0.18um CMOS technology, and include delay cells, bias circuitry, and tuning circuitry.

2.0 Initial Design based on Hand Calculations

As required, the VCO is designed in 0.18um CMOS technology. The technology-specific parameters used in all calculations are listed below:

Table 1: CMOS 0.18um Parameters

	PMOS	NMOS
V_t	0.437V	0.445V
k	92.2 uA/V^2	388 uA/V^2
c_{ox}	$c_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-12}}{4.08 \times 10^{-9}} = 8.455 \times 10^{-3} F$	

A saturated delay cell is required to generate a large oscillating voltage swing, while using a low voltage rail of 1.8V. Hence, the slow-slewing saturated delay cell shown in Figure 1 below was chosen, over its more complicated fast-slewing counterpart. The overall architecture consisting of the bias circuitry, delay cell, and tuning circuit can be found in figure 8.18 on page 337 of *VLSI for Wireless Communications* [1].

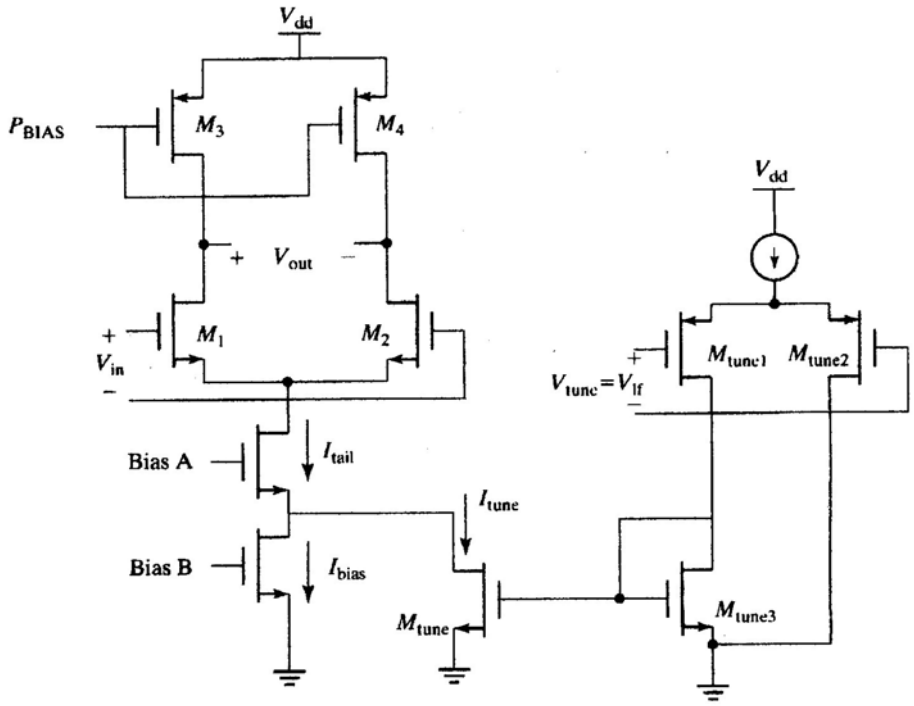

Figure 1: Slow-slewing Saturated Delay Cell [1]

2.1 Design of Delay Cell

Following the steps from section 8.4.2 of *VLSI for Wireless Communications* written by Professor Bosco Leung, we chose N = 3 to minimize the number of components used. We will design the VCO to consume 9mW, to allow for extra performance and margin from the specified 18mW. Using the formula for power specification,

Power = N x I_{bias} x V_{dd} = 3 x I_{bias} x 1.8V = 9mW,

we obtain I_{bias} = 1.6667mA.

The voltage swing of the oscillator is determined by the resistance of M_3 biased in the triode region. We wish to obtain a swing of 1V. Hence, the equivalent resistance required is given by,

$$R_{M3} = \frac{V_{swing}}{I_{biasx}} = \frac{1V}{1.6667mA} = 600\Omega$$

Now, we can determine the size ratio $(W/L)_3$ of M_3. Since M_3 is to be biased in triode, we use the triode equation

$$R_{M3} = \frac{1}{k_p\left(\frac{W}{L}\right)_3\left(|V_{GS3}| - |V_{tp}| - |V_{DS3}|\right)}.$$

V_{GS3} must be high to bias M_3 in deep triode, hence, an initial value of $|V_{GS3}| = 1.2V$ is chosen. When M_3 is biased at the midpoint of the V_{ds3} vs. I_{d3} curve, $|V_{DS3}| = V_{swing}/2 = 0.5V$. Substituting all values in the above equation, we obtain $(W/L)_3 = (12.371um/0.18um)$

The frequency of the VCO depends on the width of the source coupled pair, M1 and M2 of the delay cell. In general,

$$f_o = \frac{1}{2Nt_p}, \text{ where } t_p = RC_l \times \ln 2$$

C_l is the loading capacitance, and its value depends on the size of the source coupled pair in the current delay cell, the size of the SC pair in the next delay cell, and the size of the triode-biased PMOS, M_3. .

$$C_l = \frac{1}{2NRf_o \ln 2} = \frac{1}{2 \cdot 3 \cdot 1.9GHz \cdot 600\Omega \cdot \ln 2} = 0.21092\,pF$$

Since the size of the SC pair in the next delay cell dominates the contribution to C_l, we will approximate $C_l \cong C_{gs}$ (M_1) as an initial approximation.

$C_{gs}(M_1) = W_1 \text{ x } L_1 \text{ x } C_{ox} = W_1 \text{ x } 0.18um \text{ x } 8.445x10^{-3} = 0.21092pF.$

Hence, $(W_1/L_1) = (138.59um/0.18um)$

2.2 Design of Bias Circuitry

A replica bias scheme is implemented to maintain a constant V_{swing}. Although the design of a replica bias is more complicated than a constant bias scheme, the use of a replica bias allows the VCO to be less susceptible to process variations, noise on the power supply, and temperature variations. This is accomplished by designing PBIAS to fluctuate correspondingly with I_d of M_3, and NBIAS to fluctuate correspondingly with I_{bias}. In other words, a replica bias ensures the voltage drop across M_3 and M_4, and the voltage drop across the current source to remain at a constant, despite fluctuations in I_{tail}. Since

the VCO is designed to operate at a high frequency within a narrow frequency range, a replica bias is essential for a robust design.

Since a low voltage rail of 1.8V is used, we are unable to design a cascoded NMOS current source in the delay cell. Hence, we have only used one NMOS to create a current source. The approximations and hand calculations used in designing the bias circuitry are as follows:

Referring to Figure 8.18 of *VLSI for Wireless Communications*, and applying a simple KVL in the bias circuitry, we obtain

$V_{dd} - V_{gs9} - V_{gs14} = RI_{bias}/2$

Since we know M_3 must be in deep triode, we set V_{gs9} = 1.15V much larger than V_{gs14}=0.55V, which is just enough to turn M_{14} on. Hence,

$R = 180.18\Omega$

$V_{ov9} = V_{gs9} - V_{tp} = 1.15V - 0.437V = 0.713V$

$V_{ov14} = V_{gs14} - V_{tn} = 0.55V - 0.445V = 0.105V = V_{ov6}$

$M_{14,}$ $M_{9,}$ and M_6 must be in saturation. Hence, we can use the following formulas to determine the size of all three transistors.

$$\frac{I_{bias}}{2} = k_n \left(\frac{W}{L}\right)_{14} V_{ov_{14}}^2$$

$$\frac{I_{bias}}{2} = k_p \left(\frac{W}{L}\right)_{9} V_{ov9}^2$$

$$I_{bias} = k_n \left(\frac{W}{L}\right)_{6} V_{ov6}^2 .$$

The calculated sizes are $(W/L)_{14}$ = (70.137um/0.18um), $(W/L)_9$ = (6.4um/0.18um), and $(W/L)_6$ = (140.21um/0.18um). Note that the sizes of M_{14} and M_6 are especially large in order to keep both transistors in saturation with a low V_{gs} of 0.55V.

Hence, the PBIAS = $V_{dd} - V_{gs9}$ = 1.8V – 1.15V = 0.65V and NBIAS = V_{gs14} = 0.55V.

2.3 Design of Tuning Circuitry

We chose $V_{tune\_max} = 1V$ and $V_{tune\_min} = 0V$ for ease of use. The corresponding gain of the VCO is given by

$$K_{vco} = \frac{df_o}{dV_{tune}} = \frac{f_{\max} - f_{\min}}{V_{tune\_\min} - V_{tune\_\max}} = \frac{1.9GHz - 1.884GHz}{0V - 1V} = -16MHz/V$$

To build a safety margin, we set $K_{vco} = -22MHz/V$.

The size of M_7 and M_8 can be determined by the following relation

$$GM_{7-8} = \frac{K_{VCO} \times \left(|V_{GS3}| - |V_{tp}| - |V_{DS3}|\right)}{-f_o \times R_{M3}} = \frac{-22MHz/V(1.8V - 0.437V - 0.5V)}{-1.9GHz \cdot 600\Omega} = 16.6544uA/V$$

Hence,

$I_{tune\_max} = 16.65uA/V \times 1V = 16.65uA$

Since I_{tune_bias} must be larger than I_{tune_max}, we set $I_{tune\_bias} = 20uA$.

Finally, to determine the size of M_7 and M_8,

$$GM_{7-8} = \sqrt{I_{tune\_bias} \times k_n \times \left(\frac{W}{L}\right)_7} = \sqrt{20uA \times 92.2uA \times \left(\frac{W}{L}\right)_7} = 16.6544uA/V$$

$(W/L)_7 = 0.1504 = (0.027um/0.18um)$

However, the minimum width allowed for 0.18um technology is 0.3um. Hence, we will scale W_7 up by a factor of 10, and adjust the gain of the current mirror M_{11} to M_{12} to obtain the correct I_{tune_bias}.

Since M_7 and M_8 were scaled by a factor of 10, we must scale I_{tune_bias} also by a factor of 10, and design $10(W/L)_{11} = (W/L)_{11}$ to obtain the appropriate I_{tune}. The size of the PMOS current source of the tuning circuit is obtained by

$$I_{tune\_bias} = \frac{k_p}{2}\left(\frac{W}{L}\right)_{Ptune\_bias} (|V_{gs}| - |V_{tp}|)^2$$

where $I_{tune\_bias} = 10 \times 20uA = 200uA$, $|V_{gs}| = |PBIAS - V_{dd}| = |0.65V - 1.8V| = 1.15V$. Therefore, $(W/L)_{Ptune\_bias} = (1.53um / 0.18um)$. For M_{11} and M_{12}, we arbitrarily choose $(W/L)_{11} = 0.3um$ and $(W/L)_{12} = 3um$.

2.4 Summary of Hand Calculations

Table 2 summarizes the sizes obtained by hand calculations. All transistor lengths are at a minimum of 0.18um.

Table 2: Summary of Hand Calculations

		Calculated
Delay Cell	I_{bias}	1.67mA
	SCL pair - W_1 , W_2	138.59um
	Triode resistance – W_3	12.371um
	I_{tail} Current Source – W_6	140.21um
	I_{tune} Current Mirror – W_{11}	0.3um
Bias Circuitry	PBIAS	0.65V
	NBIAS	0.55V
	PMOS – W_9	6.4um
	NMOS - W_{14}	70.37um
	Resistor – R	180.18Ω
Tuning Circuitry	I_{tune_bias}	200uA
	Current Source - W_{tune_bias}	1.53um
	SCL pair - W_7, W_8	0.3um
	Current Mirror – W_{12}	3um

3.0 Circuit Implementation

The calculated sizes summarized in Table 2 are used in our initial simulation. However, we made significant modifications based on parametric simulation results. The modifications made and the actual implementation of the VCO is discussed in this section of the report.

Figure 2 shows the schematic of the VCO in Cadence. According to the previous section, the VCO is composed of three delay cells, a bias block, and a tuning block.

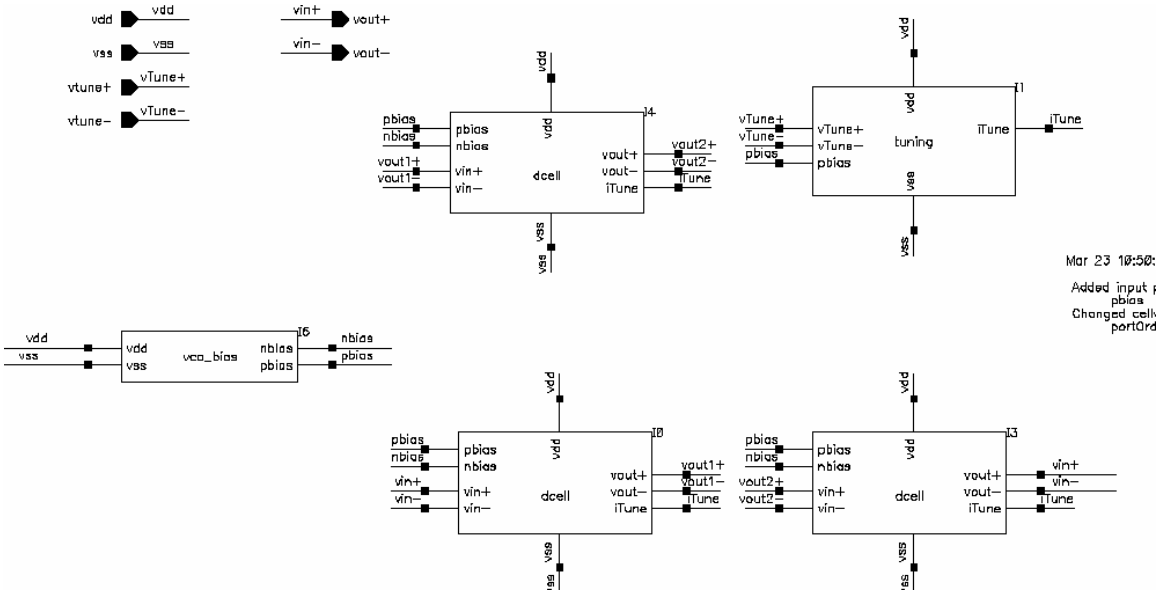

Figure 2: VCO Schematic

3.1 Implementation of Delay Cell

Firstly, we reduced I_{bias} to approximately 380uA in an attempt to reduce the large size of W_6. Therefore, we divided all sizes in the delay cell by a factor of 4.4 to maintain the previously calculated ratios. With a simple parametric analysis, we increased W_6 from 31.9um to 40um to obtain an I_{bias} of ~380uA. The increase in size of W_6 is required since the simulated NBIAS value is 0.5381V, which is lower than the calculated value of 0.55V.

Table 3: Revision of Delay Cell Calculated Sizes

Delay Cell	Calculated	Div by 4.4	Actual
I_{bias}	1.67mA	379uA	378uA
SCL pair - W_1 , W_2	138.59um	31.5um	16.55um
Triode resistance – W_3	12.371um	2.81um	2.8um
I_{tail} Current Source – W_6	140.21um	31.9um	40um
I_{tune} Current Mirror – W_{11}	0.3um	0.3um	2um

Furthermore, the frequency of oscillation was only 1GHz with the calculated W_1 of 31.5um. This deviation is expected since we grossly estimated the loading capacitance, C_l, to equal C_{gs} ($M_{1\ of\ the\ next\ delay\ cell}$) only, and neglected the capacitances introduced by

M_1 and M_3 of the current delay cell. Therefore, we reduced W_1 to 16.55um to reach a frequency oscillation of 1.9GHz.

We will discuss the change in size of W_{11} in section 3.3. Figure 3 shows the schematic of the delay cell.

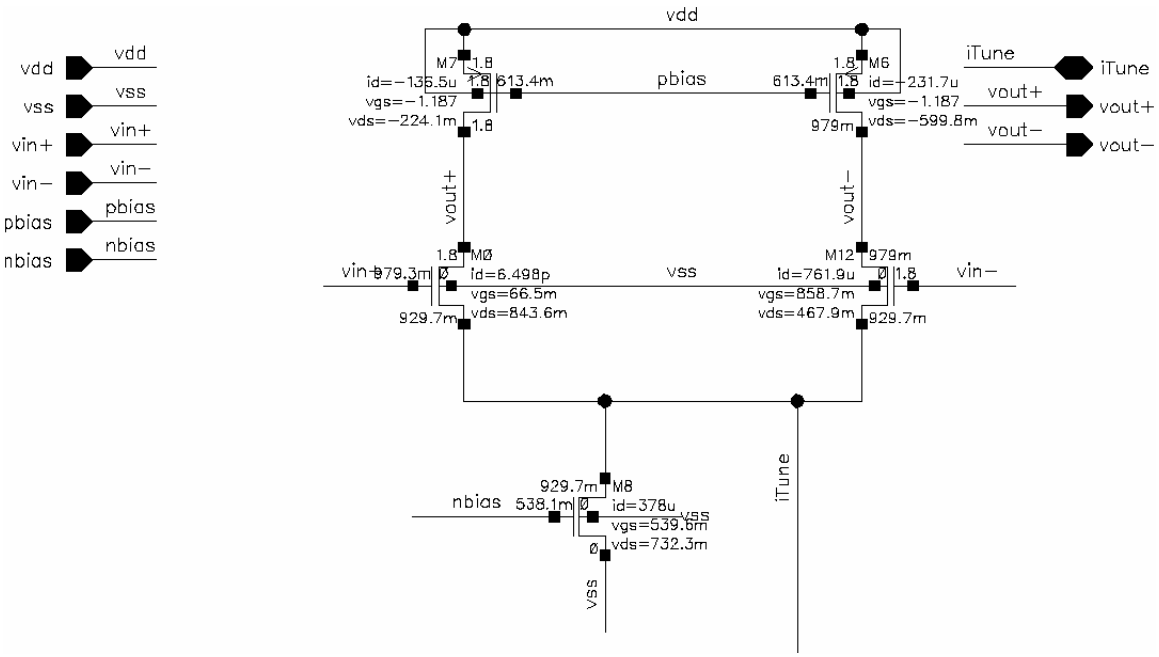

Figure 3: Delay Cell Schematic

3.2 Implementation of Bias Circuitry

When we first simulated the calculated sizes, we did not obtain the PBIAS and NBIAS voltages we designed for. Hence, we adjusted the widths of M_9 and M_{14} in order to arrive at closer bias voltages. As a result, we sized both M_9 and M_{14} down by approximately 66% to obtain the actual sizes listed in Table 4 below. The resistance value is unchanged. The bias voltages are now favourably closer to the design values. Figure 4 shows the bias circuitry schematic in Cadence.

Table 4: Revision of Bias Circuitry Calculated Sizes

Bias Circuitry	Calculated	Actual
PBIAS	0.65V	0.6134V
NBIAS	0.55V	0.5381V
PMOS – W_9	6.4um	4.26um
NMOS - W_{14}	70.37um	46.7um
Resistor – R	180.18Ω	180.2Ω

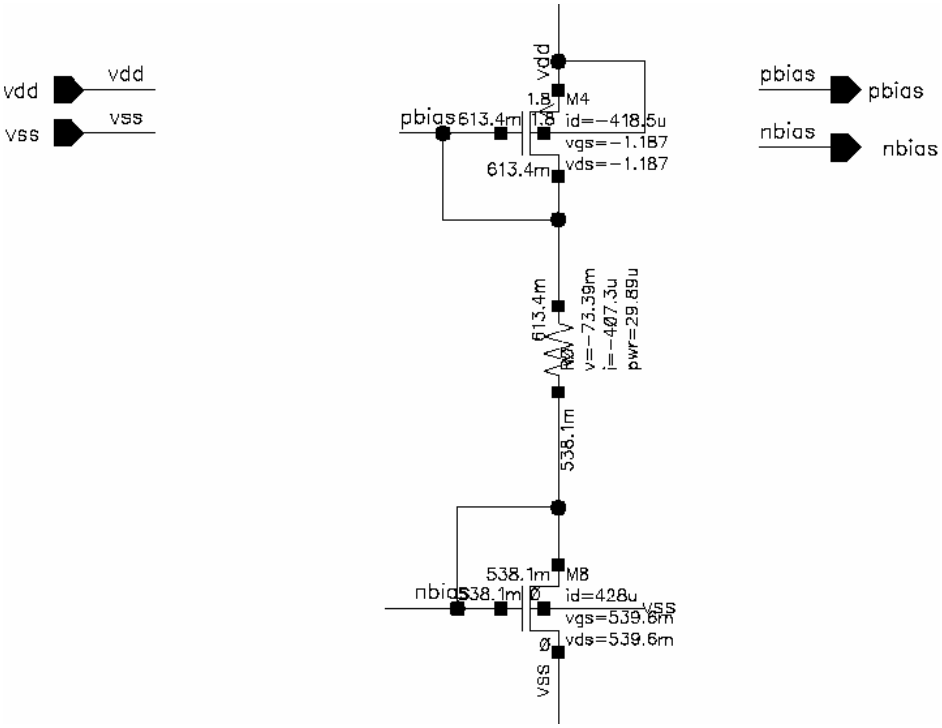

Figure 4: Bias Circuitry Schematic

3.3 Implementation of Tuning Circuitry

From Section 2.3, the design specifications of our tuning circuitry are as follows:

$V_{tune+} = 0$, $V_{tune-} = 0$ 1.9GHz

$V_{tune+} = 1V$, $V_{tune-} = 0$ 1.884GHz

The sizes of the transistors in the tuning circuitry were changed most significantly. Table 5 shows the hand calculated sizes, sizes of the first implementation, and sizes of the final tuning circuitry. We first simulated the hand calculated sizes. However, the frequency sweep was smaller than the designed 1.9GHz – 1.884GHz = 0.016Hz. Therefore, we increased W_{12} to 0.45um and W_{11} to 0.4um.

Table 5: Revision of Tuning Circuitry Sizes

Tuning Circuitry	Hand Calculated	First Implementation	Final Value
I_{tune_bias}	200uA	82uA	129.4uA
Current Source - W_{tune_bias}	1.53um	1.53um	10um
SCL pair - W_7, W_8	0.3um	0.3um	0.3um
Current Mirror – W_{12}	3um	0.45um	3um
I_{tune} Current Mirror – W_{11}	0.3um	0.4um	2um

With the first implementation, we achieved the correct frequency of oscillation at both endpoints, which is 1.9GHz at $V_{tune+} = 0$ and 1.884GHz at $V_{tune-} = 0$. The dotted line in figure 5, however, shows that the frequency versus V_{tune+} curve is totally nonlinear, in an unpredictable pattern. The unpredictable behaviour can be explained by the low I_{tune} currents utilized from $V_{tune+} = 0.5V – 1V$. The low currents cause the tuning circuit to be greatly susceptible to noise, resulting in unstable performance.

Therefore, we increased all transistor sizes in the tuning circuitry to the values in the far right column of Table 5. The I_{tune_bias} is now 129.4uA, much closer to the intended 200uA. The tuning circuit performance is now much more linear, as shown by the solid line in figure 5. The I_{tune} versus V_{tune} curve in figure 6 shows higher current levels, and also confirms improved linearity as V_{tune+} approaches 1V. It is now possible to tune the frequency of oscillation between 1.884GHz and 1.9GHz in incremental steps, when V_{tune+} is varied between 0V and 1V and V_{tune-} is kept constant at 0V. The schematic of the final tuning circuitry is shown in figure 7.

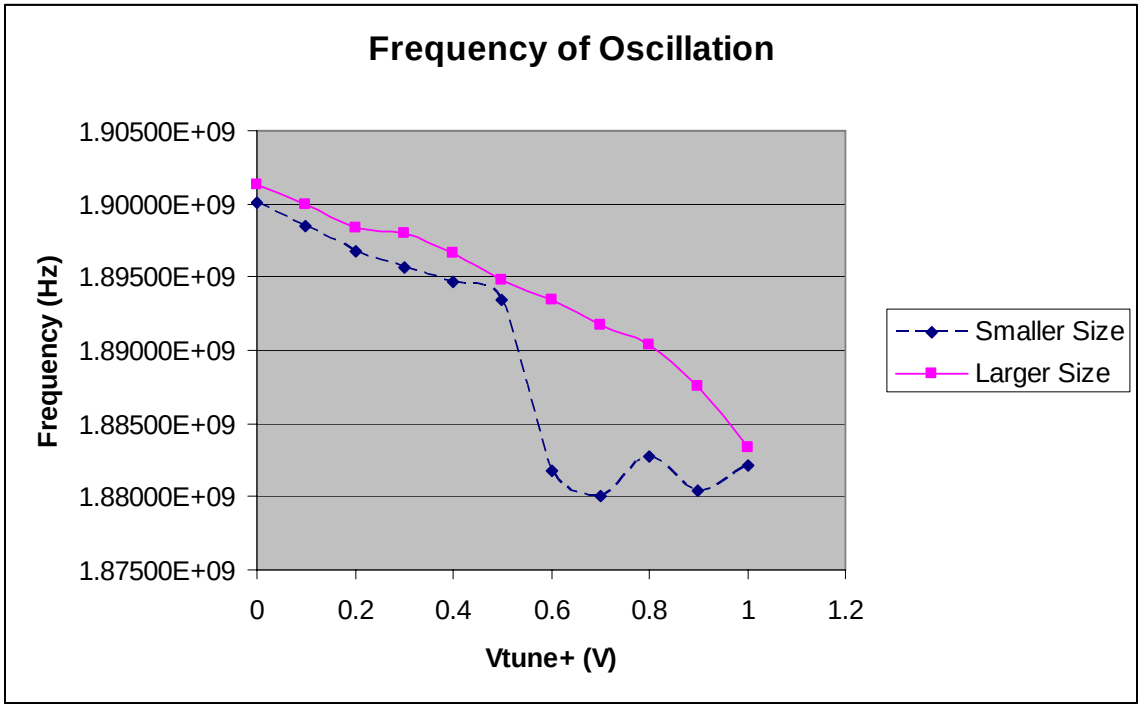

Figure 5: Frequency of Oscillation versus Tuning Voltage

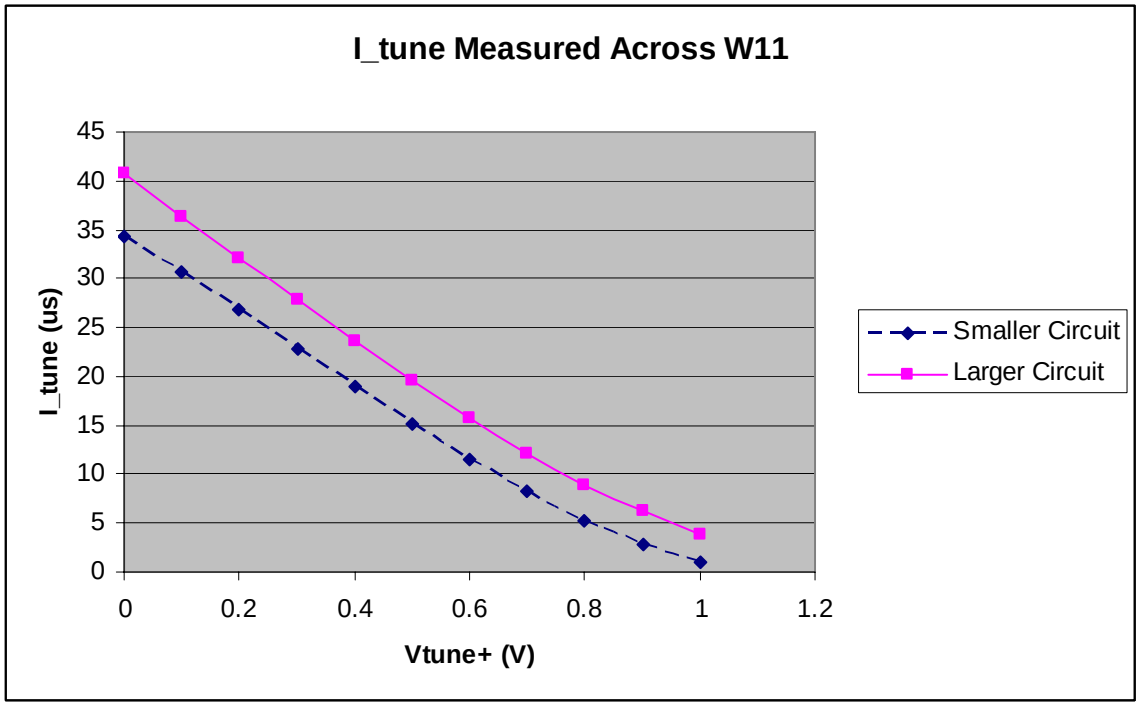

Figure 6: Frequency of Oscillation versus Tuning Voltage

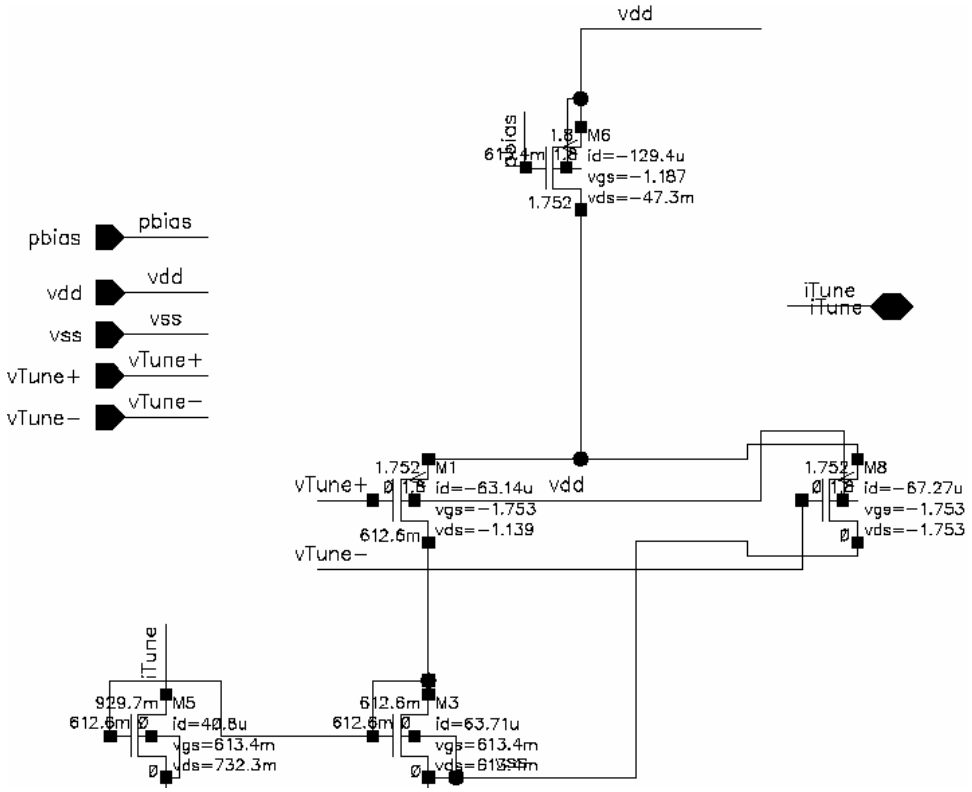

Figure 7: Tuning Circuitry Schematic

4.0 Circuit Simulation Results

Figure 8 shows the differential waveform (V_{out+} - V_{out-}) of the VCO output, and figure 9 shows the two single-ended V_{out+} and V_{out-} waveforms. The voltage swing is almost 1V, as designed.

The frequency of oscillation and the performance of the tuning circuit was thoroughly described in section 3.3. In summary, the frequency of oscillation with V_{tune+} = V_{tune-} = 0V is 1.9001GHz and with V_{tune+} = 0.9V and V_{tune-} = 0V is 1.884GHz. The voltage swing is unchanged as the frequency changes from 1.884GHz to 1.9GHz.

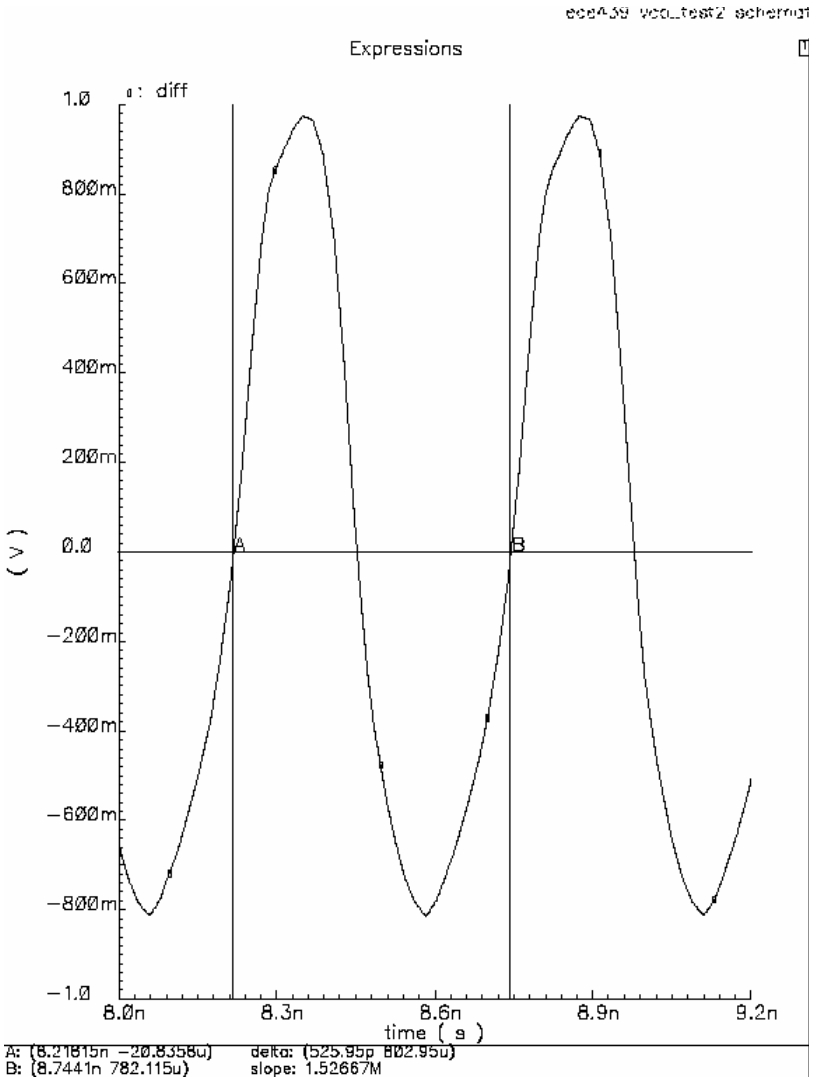

Figure 8: Differential Swing of VCO Output

The power consumption of the entire VCO is only 3.204mW at the peak frequency of 1.9GHz. The simulated power consumption is significantly lower than the project specification of 18mW.

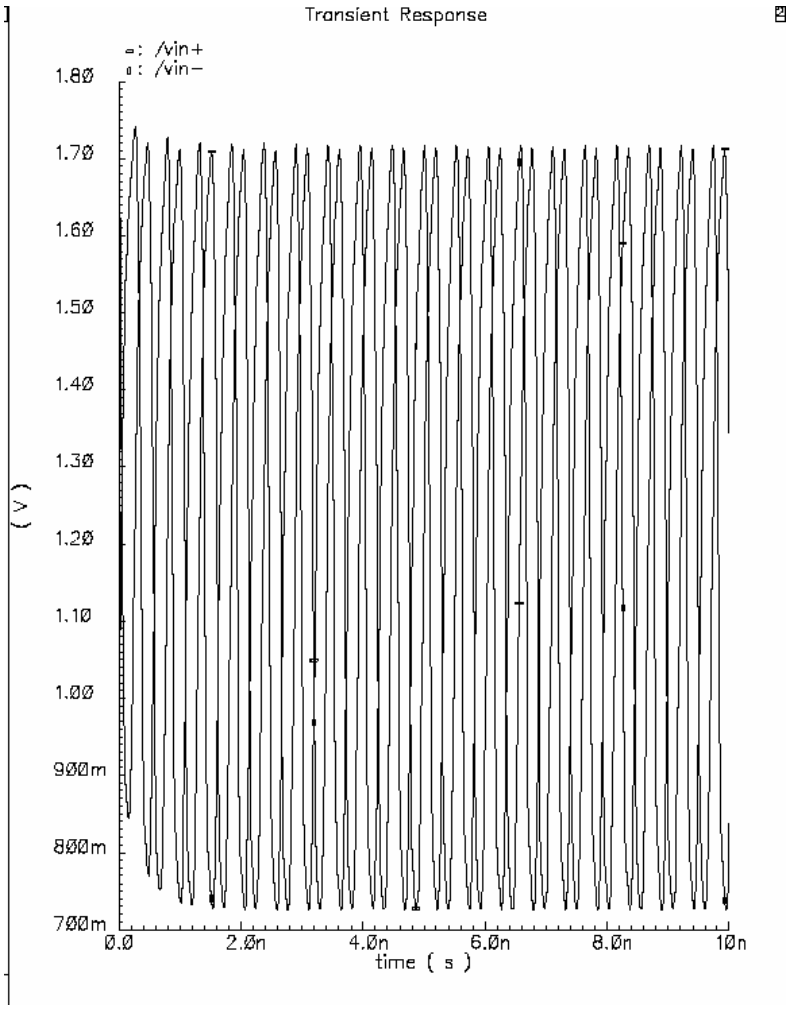

Figure 9: Single-Ended Swing of VCO Output

5.0 Layout

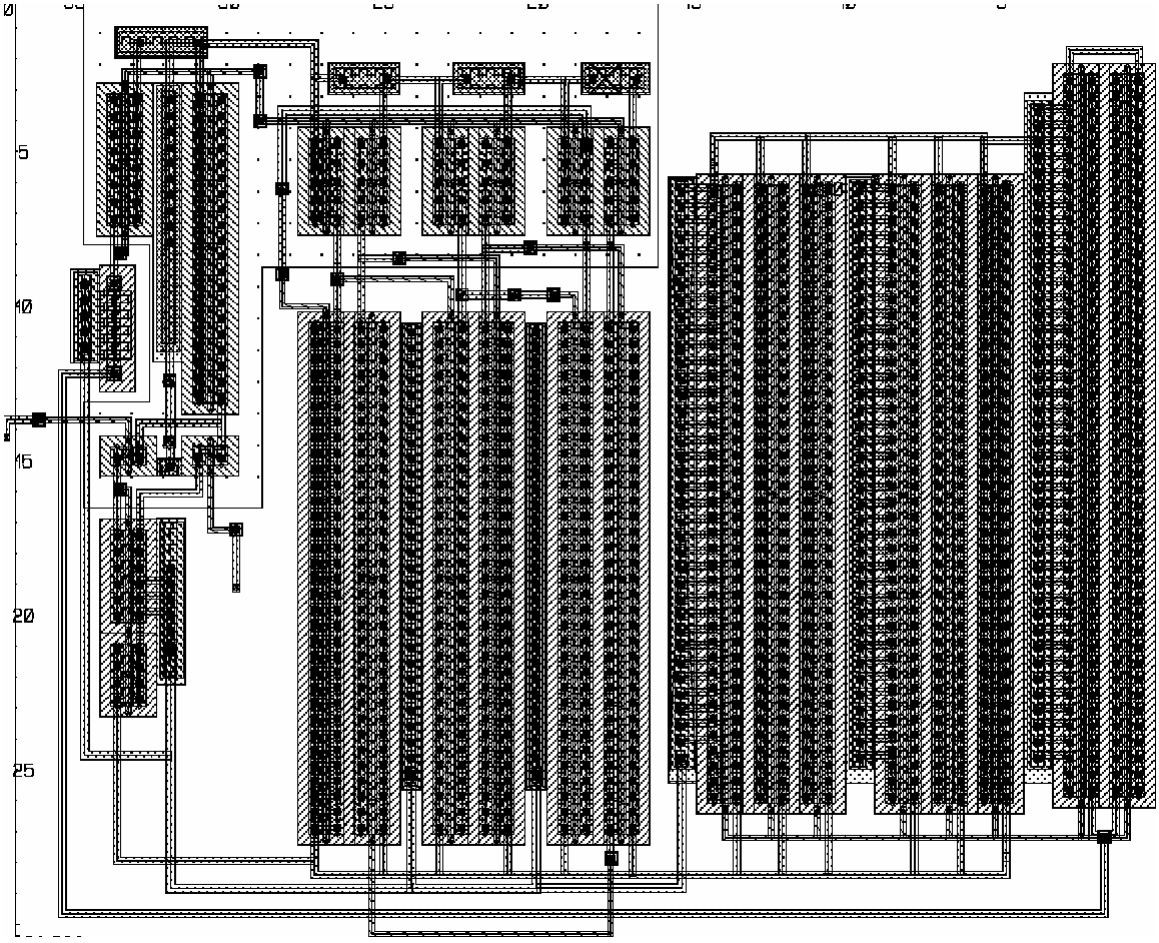

Figure 10: Layout of VCO

The layout of the cell measures 35.72m x 29.80um. To save time, we utilized the ready-made transistor from the CMCpcells library to layout the circuit. We originally intended to use poly resistors to layout the resistance of 180.2Ω in the bias circuitry. However, the resistance is too low for a poly resistor, and we resolved to use an N-implant resistor, due to its lower sheet resistance.

In additions, this layout utilizes two metal layers to provide connections to the metal contacts. As for body contact sharing, all transistors require a connection to a voltage biased body contact. For PMOS transistors, the body is of N-type and connected to VDD. For NMOS transistor, the body is of P-type and grounded. DRC allows transistors

to share a body contact as long as the contact is within 5 μm from the body. Hence, we can reduce the number of body contacts in the layout by sharing between transistors.

The following is an excerpt from the built-in DRC test in Cadence. The excerpt shows that our layout has successfully passed the DRC test.

```
\o DRC started at Sun Mar 27 22:35:47 2005
\o
\o Validating hierarchy instantiation for:
\o library: ece439
\o cell:    final_vco
\o view:    layout
\o Rules come from library cmosp18.
\o Rules path is divaDRC.rul.
\o Inclusion limit is set to 1000.
\o Running layout DRC analysis
\o Flat mode
\o Full checking.
\o executing: rw = geomAndNot(geomAndNot("dnw" "nwell") "drcex")
.
.
.
\o DRC started.......Sun Mar 27 22:35:47 2005
\o     completed ....Sun Mar 27 22:36:14 2005
\o     CPU TIME = 00:00:06  TOTAL TIME = 00:00:27
\o *********   Summary of rule violations for cell "final_vco layout"    *********
\o
\o    Total errors found: 0
```

6.0 Conclusion

The design of our Voltage Controlled Oscillator (VCO) was implemented using a three-stage ring oscillator. A slow-slewing saturated topology was used for all three delay cells of the ring oscillator. From circuit simulations, the oscillating voltage swing is close to 1V. The output frequency varies from 1.884GHz to 1.9GHz by adjusting the tuning voltage from 0.9V to 0V. Therefore, the simulated K_{vco} is -17.9MHz/V, which is very close to the calculated value of -16MHz/V. The power consumption is of the VCO is 3.2mW at 1.9GHz, and the total consumed cell area is 35.72m x 29.80um. Therefore, we have met or exceeded all project specifications.

7.0 References

[1] Leung, Bosco, "*VLSI for Wireless Communication*" Prentice Hall, 2002.